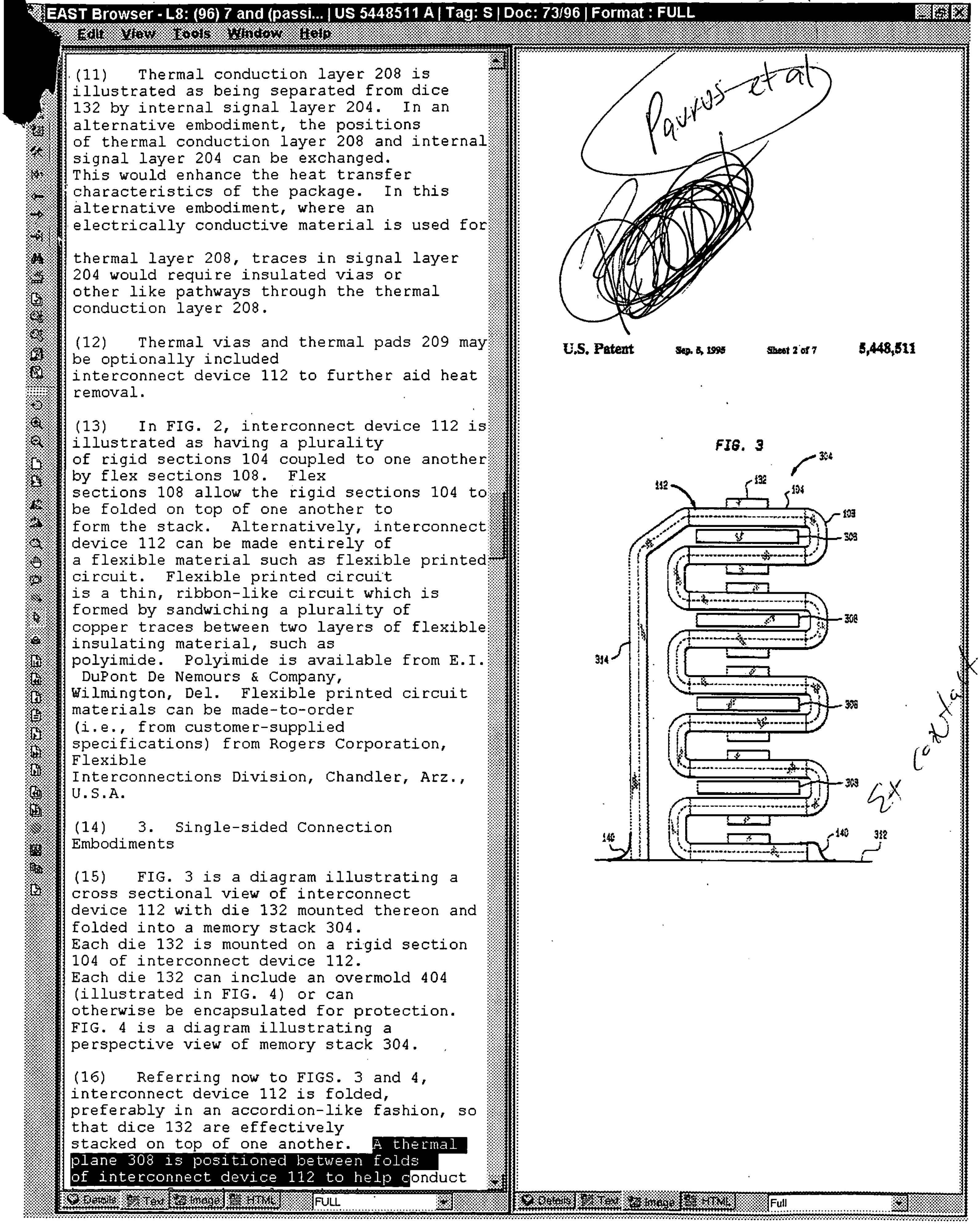

(11) Thermal conduction layer 208 is illustrated as being separated from dice 132 by internal signal layer 204. In an alternative embodiment, the positions of thermal conduction layer 208 and internal signal layer 204 can be exchanged. This would enhance the heat transfer characteristics of the package. In this alternative embodiment, where an electrically conductive material is used for

thermal layer 208, traces in signal layer 204 would require insulated vias or other like pathways through the thermal conduction layer 208.

(12) Thermal vias and thermal pads 209 may be optionally included interconnect device 112 to further aid heat removal.

(13) In FIG. 2, interconnect device 112 is illustrated as having a plurality of rigid sections 104 coupled to one another by flex sections 108. Flex sections 108 allow the rigid sections 104 to be folded on top of one another to form the stack. Alternatively, interconnect device 112 can be made entirely of a flexible material such as flexible printed circuit. Flexible printed circuit is a thin, ribbon-like circuit which is formed by sandwiching a plurality of copper traces between two layers of flexible insulating material, such as polyimide. Polyimide is available from E.I. DuPont De Nemours & Company, Wilmington, Del. Flexible printed circuit materials can be made-to-order (i.e., from customer-supplied specifications) from Rogers Corporation, Flexible Interconnections Division, Chandler, Arz., U.S.A.

(14) 3. Single-sided Connection Embodiments

(15) FIG. 3 is a diagram illustrating a cross sectional view of interconnect device 112 with die 132 mounted thereon and folded into a memory stack 304. Each die 132 is mounted on a rigid section 104 of interconnect device 112. Each die 132 can include an overmold 404 (illustrated in FIG. 4) or can otherwise be encapsulated for protection. FIG. 4 is a diagram illustrating a perspective view of memory stack 304.

(16) Referring now to FIGS. 3 and 4, interconnect device 112 is folded, preferably in an accordion-like fashion, so that dice 132 are effectively stacked on top of one another. A thermal plane 308 is positioned between folds of interconnect device 112 to help conduct

Pavrus et al

U.S. Patent Sep. 5, 1995 Sheet 2 of 7 5,448,511

FIG. 3

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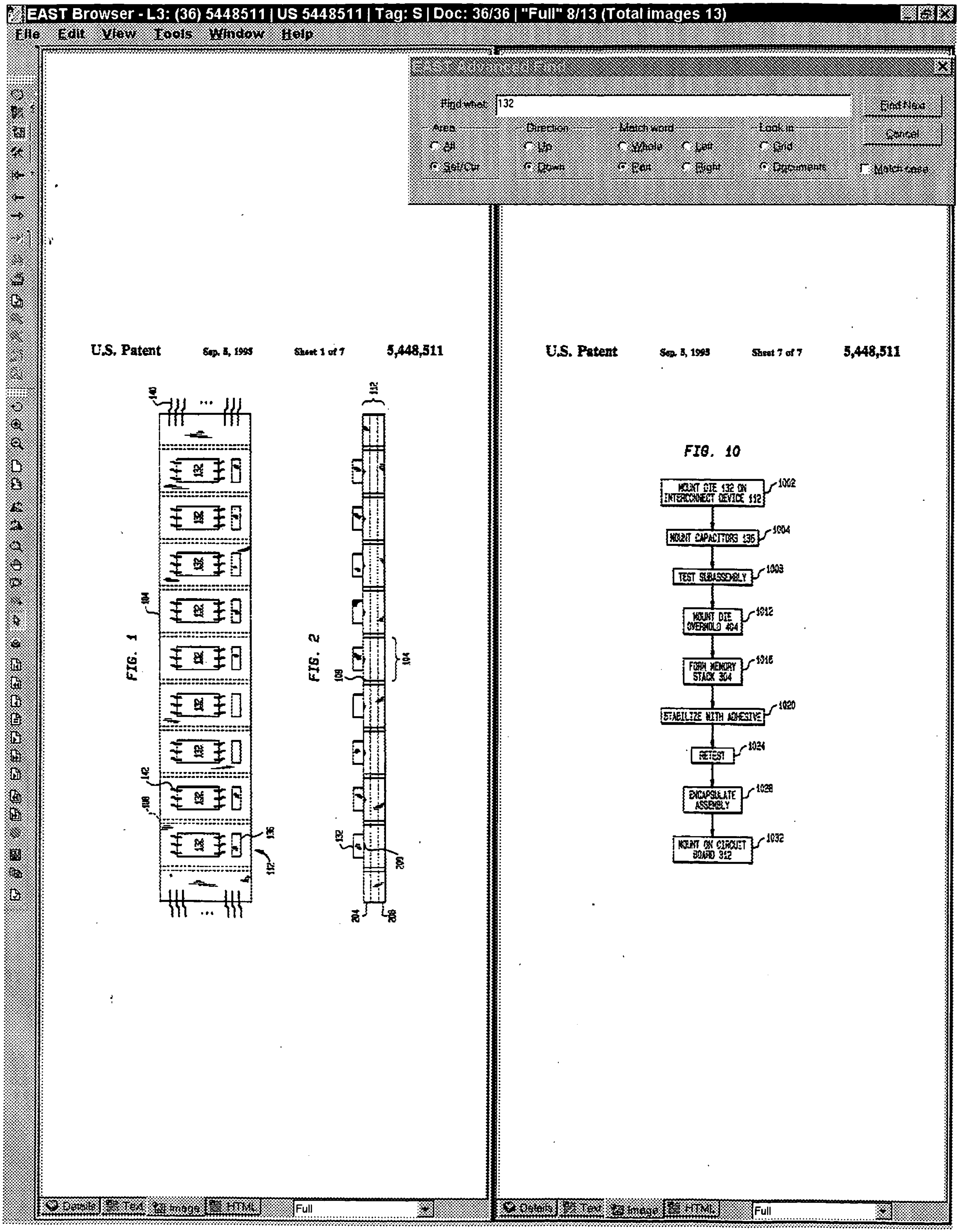

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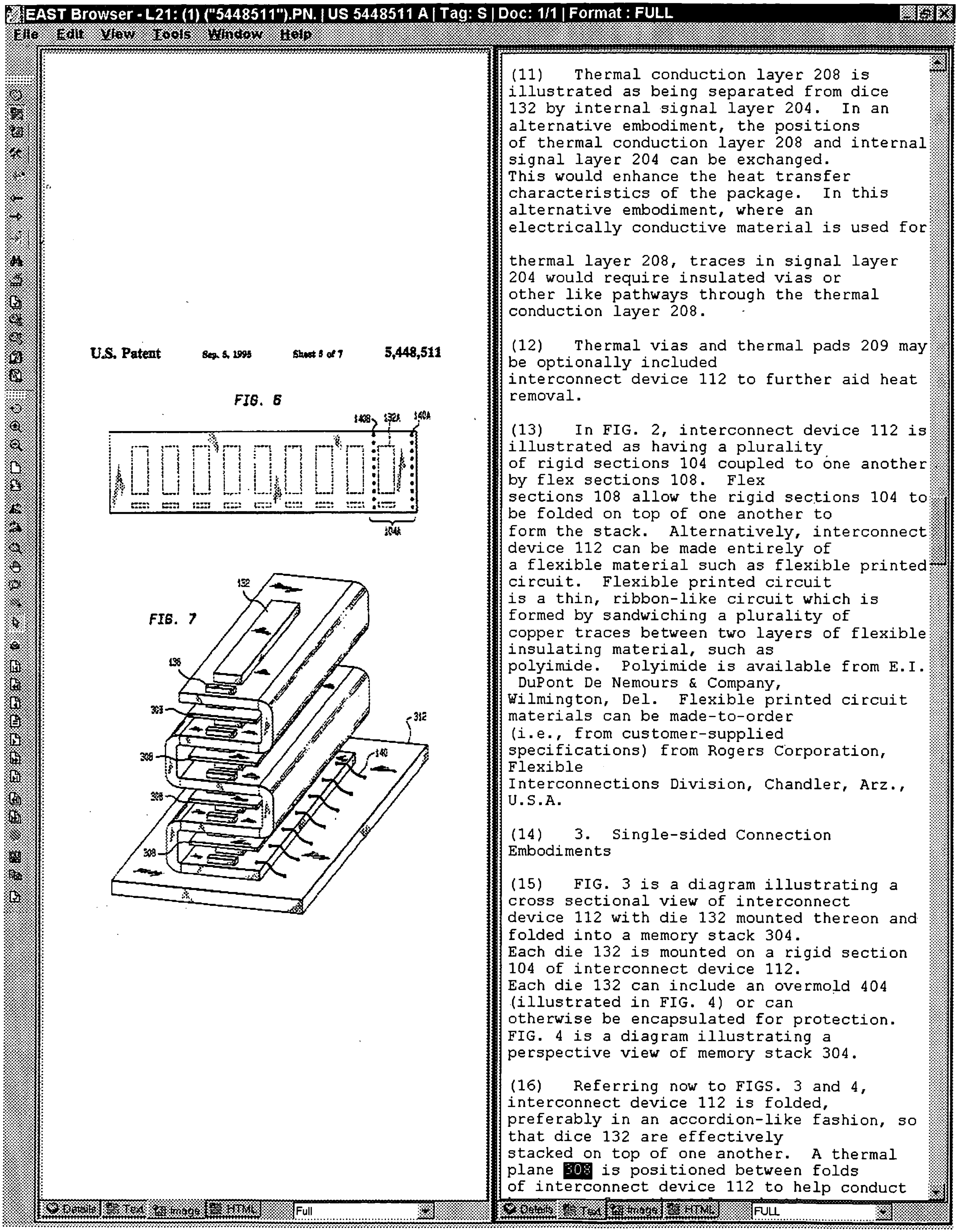

U.S. Patent Sep. 5, 1995 Sheet 5 of 7 5,448,511

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thermal layer 208, traces in signal layer 204 would require insulated vias or other like pathways through the thermal conduction layer 208.

(12) Thermal vias and thermal pads 209 may be optionally included interconnect device 112 to further aid heat removal.

(13) In FIG. 2, interconnect device 112 is illustrated as having a plurality of rigid sections 104 coupled to one another by flex sections 108. Flex sections 108 allow the rigid sections 104 to be folded on top of one another to form the stack. Alternatively, interconnect device 112 can be made entirely of a flexible material such as flexible printed circuit. Flexible printed circuit is a thin, ribbon-like circuit which is formed by sandwiching a plurality of copper traces between two layers of flexible insulating material, such as polyimide. Polyimide is available from E.I. DuPont De Nemours & Company, Wilmington, Del. Flexible printed circuit materials can be made-to-order (i.e., from customer-supplied specifications) from Rogers Corporation, Flexible Interconnections Division, Chandler, Arz., U.S.A.

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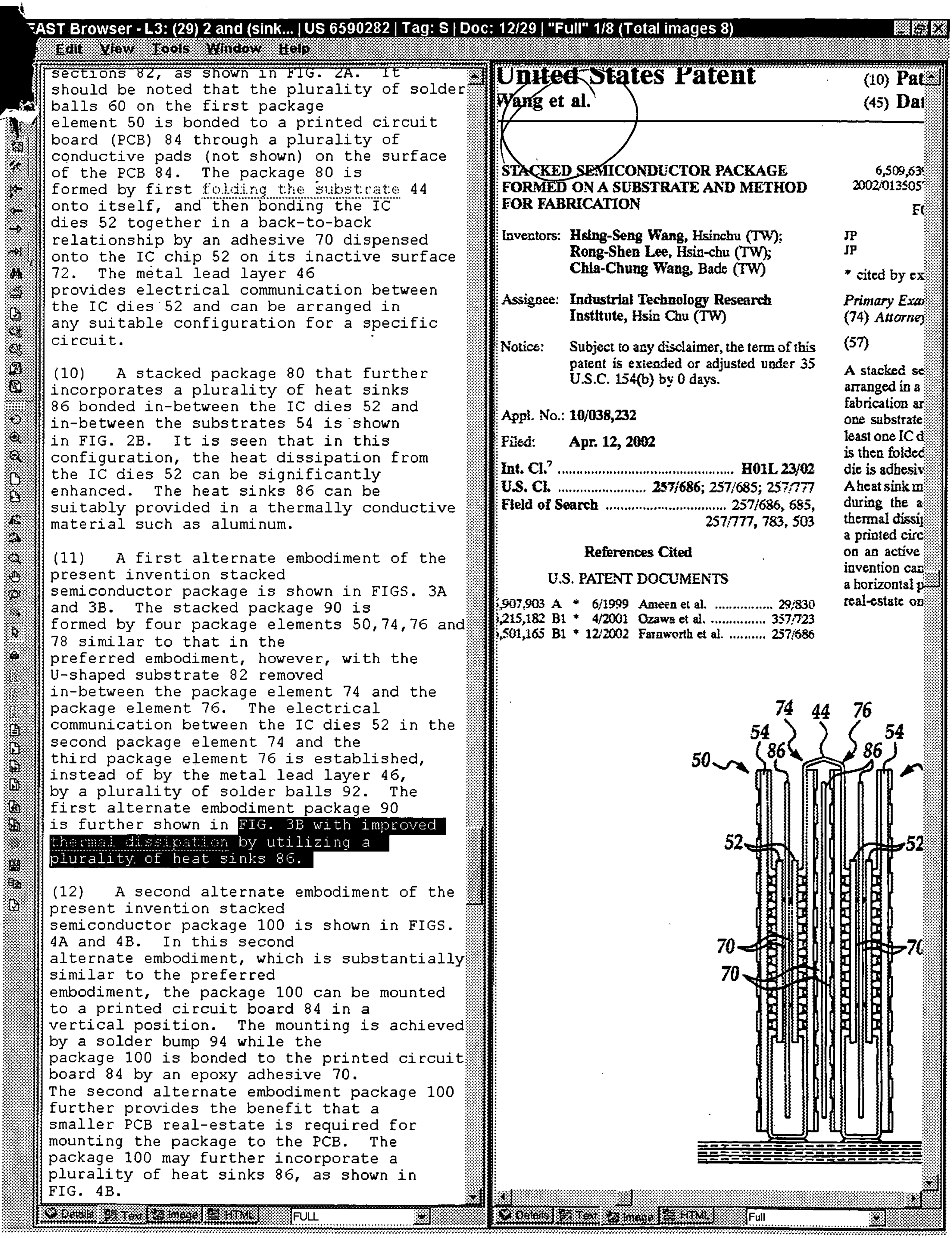

sections 82, as shown in FIG. 2A. It should be noted that the plurality of solder balls 60 on the first package element 50 is bonded to a printed circuit board (PCB) 84 through a plurality of conductive pads (not shown) on the surface of the PCB 84. The package 80 is formed by first folding the substrate 44 onto itself, and then bonding the IC dies 52 together in a back-to-back relationship by an adhesive 70 dispensed onto the IC chip 52 on its inactive surface 72. The metal lead layer 46 provides electrical communication between the IC dies 52 and can be arranged in any suitable configuration for a specific circuit.

(10) A stacked package 80 that further incorporates a plurality of heat sinks 86 bonded in-between the IC dies 52 and in-between the substrates 54 is shown in FIG. 2B. It is seen that in this configuration, the heat dissipation from the IC dies 52 can be significantly enhanced. The heat sinks 86 can be suitably provided in a thermally conductive material such as aluminum.

(11) A first alternate embodiment of the present invention stacked semiconductor package is shown in FIGS. 3A and 3B. The stacked package 90 is formed by four package elements 50,74,76 and 78 similar to that in the preferred embodiment, however, with the U-shaped substrate 82 removed in-between the package element 74 and the package element 76. The electrical communication between the IC dies 52 in the second package element 74 and the third package element 76 is established, instead of by the metal lead layer 46, by a plurality of solder balls 92. The first alternate embodiment package 90 is further shown in FIG. 3B with improved thermal dissipation by utilizing a plurality of heat sinks 86.

(12) A second alternate embodiment of the present invention stacked semiconductor package 100 is shown in FIGS. 4A and 4B. In this second alternate embodiment, which is substantially similar to the preferred embodiment, the package 100 can be mounted to a printed circuit board 84 in a vertical position. The mounting is achieved by a solder bump 94 while the package 100 is bonded to the printed circuit board 84 by an epoxy adhesive 70. The second alternate embodiment package 100 further provides the benefit that a smaller PCB real-estate is required for mounting the package to the PCB. The package 100 may further incorporate a plurality of heat sinks 86, as shown in FIG. 4B.

United States Patent

Wang et al.

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STACKED SEMICONDUCTOR PACKAGE FORMED ON A SUBSTRATE AND METHOD FOR FABRICATION

Inventors: **Hsing-Seng Wang**, Hsinchu (TW); **Rong-Shen Lee**, Hsin-chu (TW); **Chia-Chung Wang**, Bade (TW)

Assignee: **Industrial Technology Research Institute**, Hsin Chu (TW)

Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

Appl. No.: **10/038,232**

Filed: **Apr. 12, 2002**

Int. Cl.^{7} **H01L 23/02**
U.S. Cl. **257/686**; 257/685; 257/777
Field of Search 257/686, 685, 257/777, 783, 503

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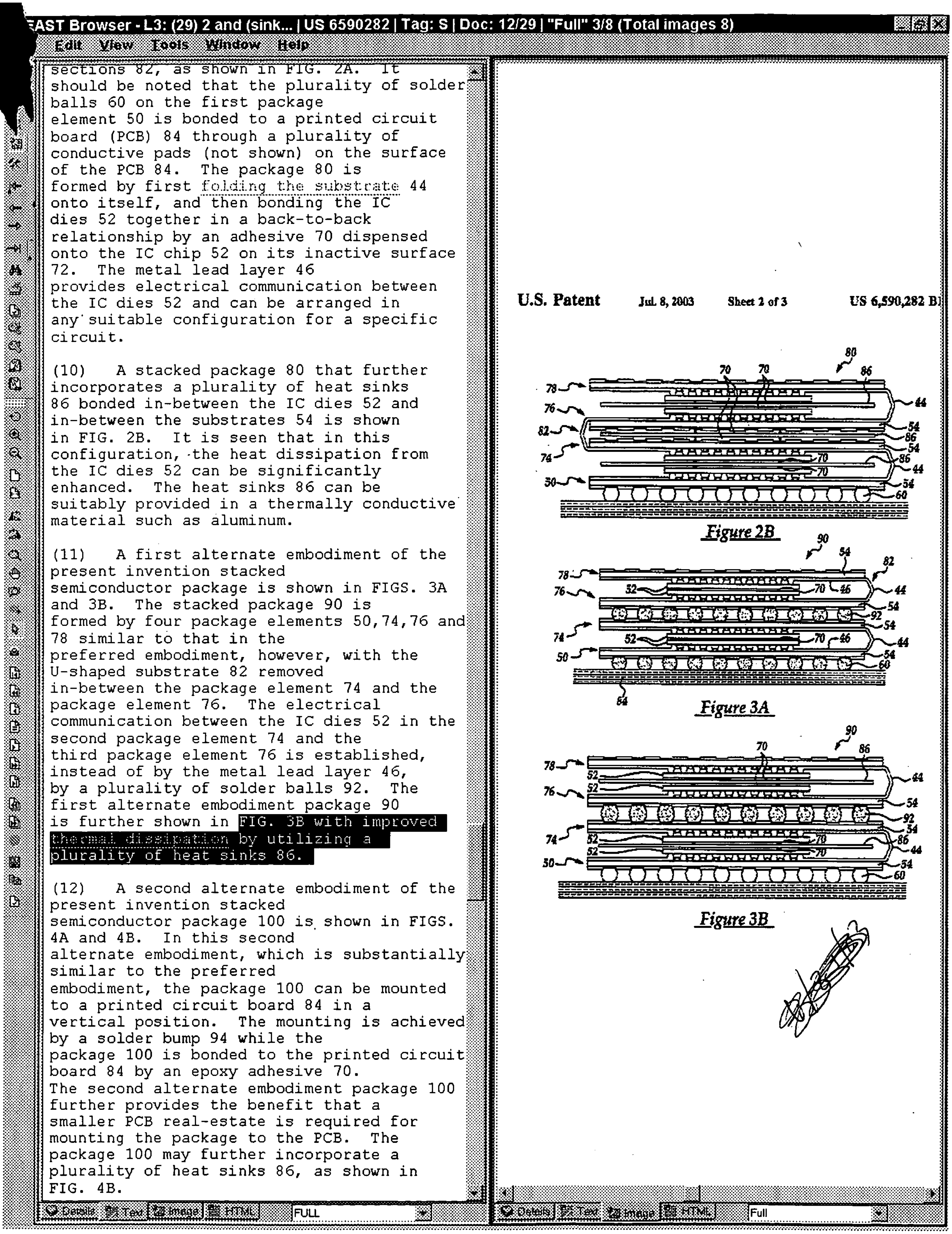

sections 82, as shown in FIG. 2A. It should be noted that the plurality of solder balls 60 on the first package element 50 is bonded to a printed circuit board (PCB) 84 through a plurality of conductive pads (not shown) on the surface of the PCB 84. The package 80 is formed by first folding the substrate 44 onto itself, and then bonding the IC dies 52 together in a back-to-back relationship by an adhesive 70 dispensed onto the IC chip 52 on its inactive surface 72. The metal lead layer 46 provides electrical communication between the IC dies 52 and can be arranged in any suitable configuration for a specific circuit.

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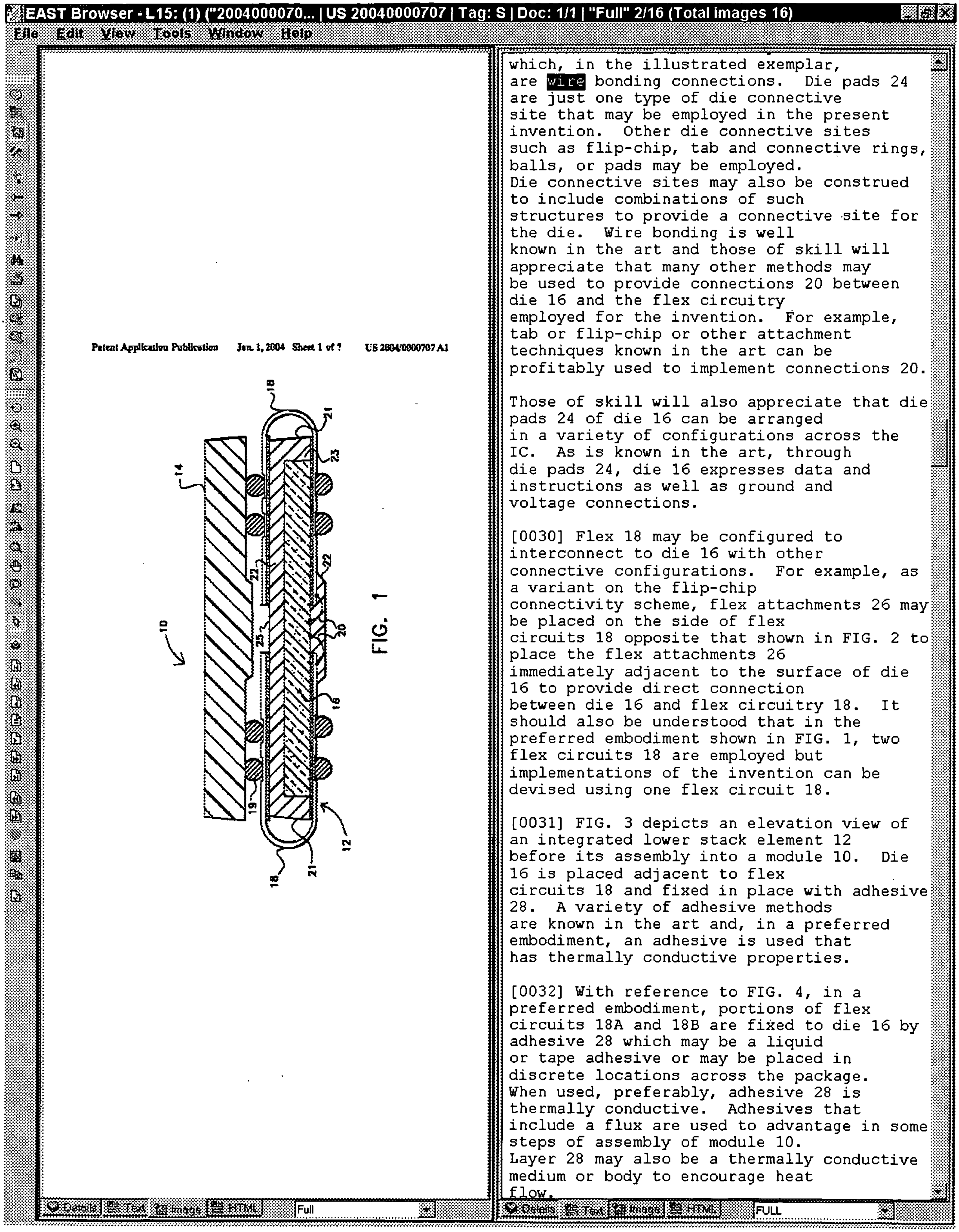
U.S. Patent Jul. 8, 2003 Sheet 2 of 3 US 6,590,282 B1

Figure 2B

Figure 3A

Figure 3B



Patent Application Publication Jan. 1, 2004 Sheet 1 of 7 US 2004/0000707 A1

FIG. 1

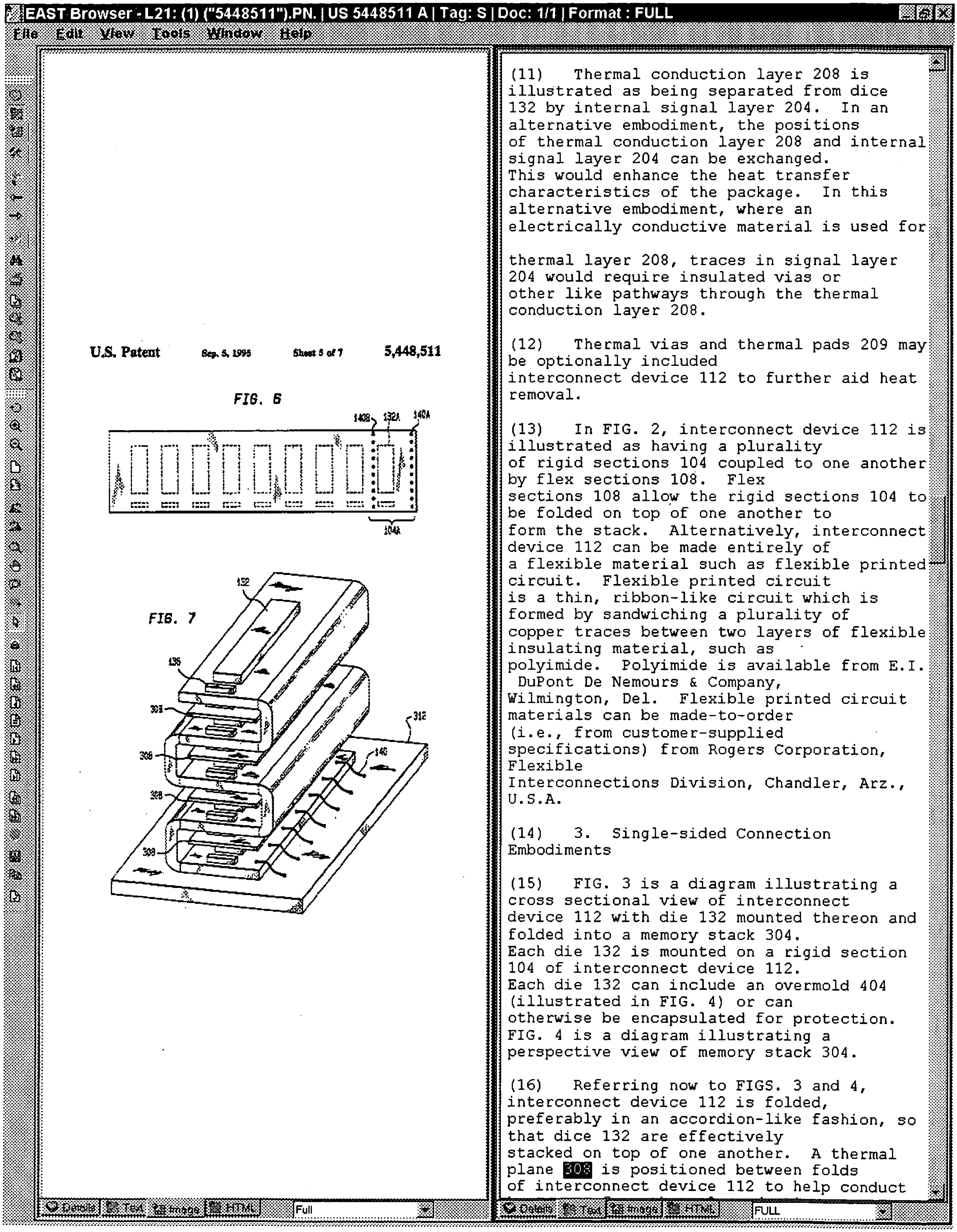
which, in the illustrated exemplar, are wire bonding connections. Die pads 24 are just one type of die connective site that may be employed in the present invention. Other die connective sites such as flip-chip, tab and connective rings, balls, or pads may be employed. Die connective sites may also be construed to include combinations of such structures to provide a connective site for the die. Wire bonding is well known in the art and those of skill will appreciate that many other methods may be used to provide connections 20 between die 16 and the flex circuitry employed for the invention. For example, tab or flip-chip or other attachment techniques known in the art can be profitably used to implement connections 20.

Those of skill will also appreciate that die pads 24 of die 16 can be arranged in a variety of configurations across the IC. As is known in the art, through die pads 24, die 16 expresses data and instructions as well as ground and voltage connections.

[0030] Flex 18 may be configured to interconnect to die 16 with other connective configurations. For example, as a variant on the flip-chip connectivity scheme, flex attachments 26 may be placed on the side of flex circuits 18 opposite that shown in FIG. 2 to place the flex attachments 26 immediately adjacent to the surface of die 16 to provide direct connection between die 16 and flex circuitry 18. It should also be understood that in the preferred embodiment shown in FIG. 1, two flex circuits 18 are employed but implementations of the invention can be devised using one flex circuit 18.

[0031] FIG. 3 depicts an elevation view of an integrated lower stack element 12 before its assembly into a module 10. Die 16 is placed adjacent to flex circuits 18 and fixed in place with adhesive 28. A variety of adhesive methods are known in the art and, in a preferred embodiment, an adhesive is used that has thermally conductive properties.

[0032] With reference to FIG. 4, in a preferred embodiment, portions of flex circuits 18A and 18B are fixed to die 16 by adhesive 28 which may be a liquid or tape adhesive or may be placed in discrete locations across the package. When used, preferably, adhesive 28 is thermally conductive. Adhesives that include a flux are used to advantage in some steps of assembly of module 10. Layer 28 may also be a thermally conductive medium or body to encourage heat flow.



U.S. Patent Sep. 5, 1995 Sheet 5 of 7 5,448,511

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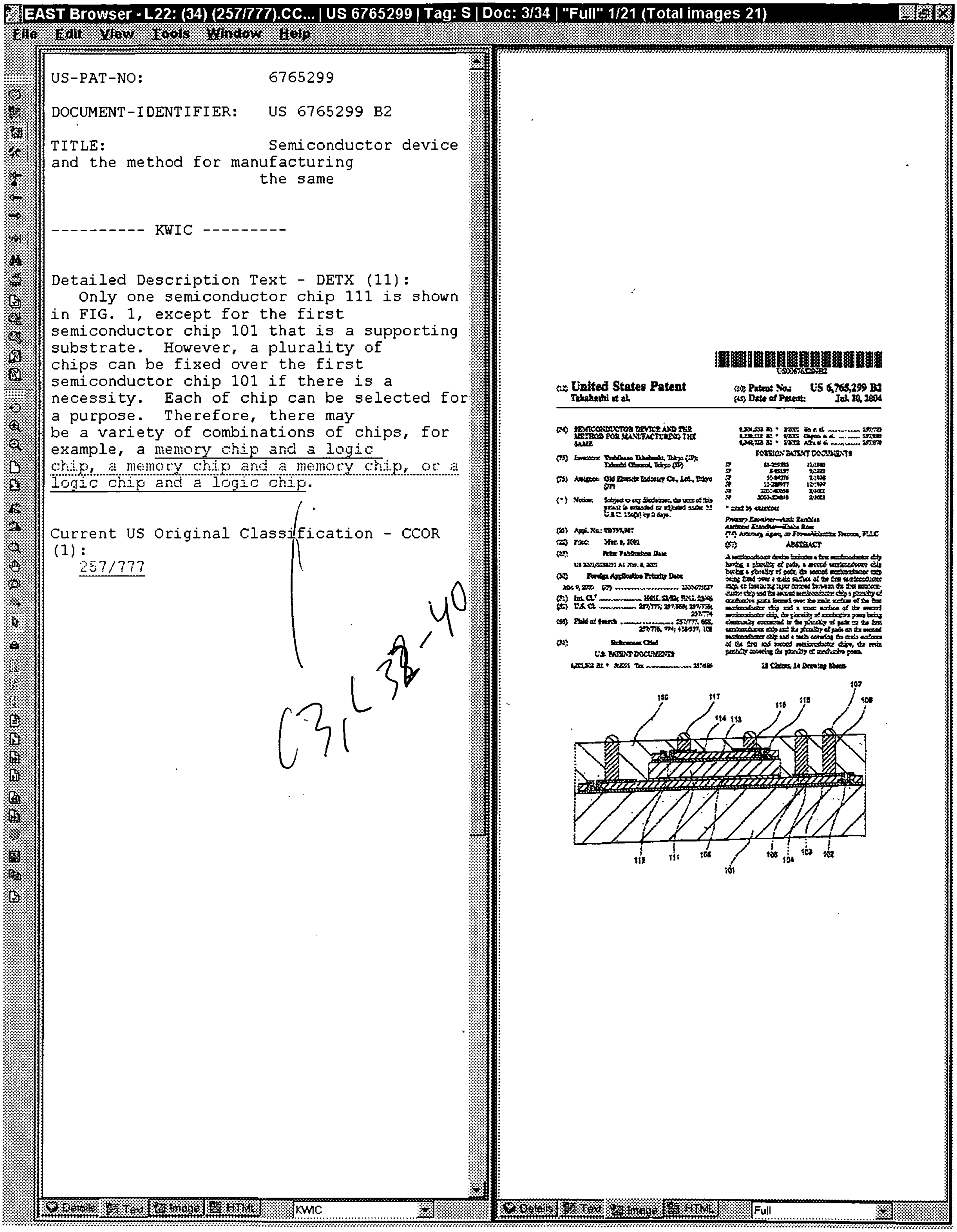


US-PAT-NO: 6765299

DOCUMENT-IDENTIFIER: US 6765299 B2

TITLE: Semiconductor device and the method for manufacturing the same

---------- KWIC ---------

Detailed Description Text - DETX (11):
Only one semiconductor chip 111 is shown in FIG. 1, except for the first semiconductor chip 101 that is a supporting substrate. However, a plurality of chips can be fixed over the first semiconductor chip 101 if there is a necessity. Each of chip can be selected for a purpose. Therefore, there may be a variety of combinations of chips, for example, a memory chip and a logic chip, a memory chip and a memory chip, or a logic chip and a logic chip.

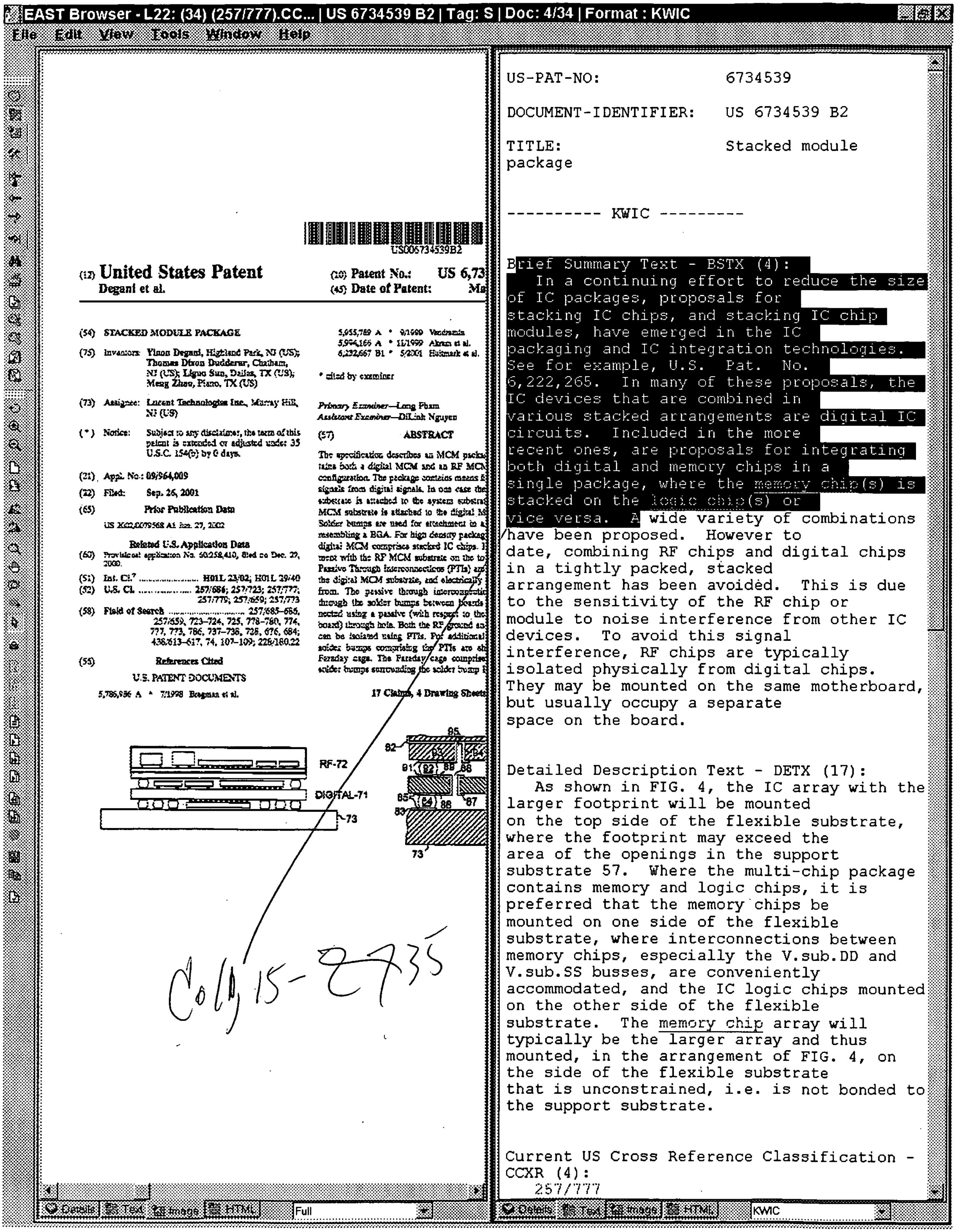
Current US Original Classification - CCOR (1):
257/777

C3, L32-40

(12) United States Patent
Takahashi et al.

(10) Patent No.: US 6,765,299 B2
(45) Date of Patent: Jul. 20, 2004

(57) ABSTRACT



US006734539B2

(12) **United States Patent**
Degani et al.

(10) **Patent No.:** **US 6,73**
(45) **Date of Patent:** **Ma**

(54) STACKED MODULE PACKAGE

(75) Inventors: Yinon Degani, Highland Park, NJ (US); Thomas Dixon Dudderar, Chatham, NJ (US); Liguo Sun, Dallas, TX (US); Meng Zhao, Plano, TX (US)

(73) Assignee: Lucent Technologies Inc., Murray Hill, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/964,009

(22) Filed: Sep. 26, 2001

(65) Prior Publication Data

US 2002/0079568 A1 Jun. 27, 2002

Related U.S. Application Data

(60) Provisional application No. 60/258,410, filed on Dec. 27, 2000.

(51) Int. Cl.^{7} H01L 23/02; H01L 29/40
(52) U.S. Cl. 257/686; 257/723; 257/777; 257/779; 257/659; 257/773
(58) Field of Search 257/685–686, 257/659, 723–724, 725, 778–780, 774, 777, 773, 786, 737–738, 728, 676, 684; 438/613–617, 74, 107–109; 228/180.22

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Primary Examiner—Long Pham
Assistant Examiner—DiLinh Nguyen

(57) ABSTRACT

The specification describes an MCM packa tains both a digital MCM and an RF MCN configuration. The package contains means f signals from digital signals. In one case the substrate is attached to the system substra MCM substrate is attached to the digital M Solder bumps are used for attachment in a resembling a BGA. For high density packag digital MCM comprises stacked IC chips. I ment with the RF MCM substrate on the to Passive Through Interconnections (PTIs) are the digital MCM substrate, and electrically from. The passive through interconnectin through the solder bumps between boards nected using a passive (with respect to the board) through hole. Both the RF ground an can be isolated using PTIs. For additional solder bumps comprising the PTIs are sh Faraday cage. The Faraday cage comprise solder bumps surrounding the solder bump f

17 Claims, 4 Drawing Sheets

Col 1, 15-27 35

US-PAT-NO: 6734539

DOCUMENT-IDENTIFIER: US 6734539 B2

TITLE: Stacked module package

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Brief Summary Text - BSTX (4):
In a continuing effort to reduce the size of IC packages, proposals for stacking IC chips, and stacking IC chip modules, have emerged in the IC packaging and IC integration technologies. See for example, U.S. Pat. No. 6,222,265. In many of these proposals, the IC devices that are combined in various stacked arrangements are digital IC circuits. Included in the more recent ones, are proposals for integrating both digital and memory chips in a single package, where the memory chip(s) is stacked on the logic chip(s) or vice versa. A wide variety of combinations have been proposed. However to date, combining RF chips and digital chips in a tightly packed, stacked arrangement has been avoided. This is due to the sensitivity of the RF chip or module to noise interference from other IC devices. To avoid this signal interference, RF chips are typically isolated physically from digital chips. They may be mounted on the same motherboard, but usually occupy a separate space on the board.

Detailed Description Text - DETX (17):
As shown in FIG. 4, the IC array with the larger footprint will be mounted on the top side of the flexible substrate, where the footprint may exceed the area of the openings in the support substrate 57. Where the multi-chip package contains memory and logic chips, it is preferred that the memory chips be mounted on one side of the flexible substrate, where interconnections between memory chips, especially the V.sub.DD and V.sub.SS busses, are conveniently accommodated, and the IC logic chips mounted on the other side of the flexible substrate. The memory chip array will typically be the larger array and thus mounted, in the arrangement of FIG. 4, on the side of the flexible substrate that is unconstrained, i.e. is not bonded to the support substrate.

Current US Cross Reference Classification - CCXR (4):
257/777